

REMARKS

Claims 36 and 37 are amended. Claims 55-60 are added. Claims 24-31, 36, 37, 39-41 and 45-60 are in the application for consideration.

Claims 36, 37, 40 and 41 stand rejected as being obvious over U.S. Patent No. 5,270,240 to Lee. The Examiner asserts that *prima facie* obviousness is established because in general the transposition of process steps, or the splitting of one step into two, does not patentably distinguish the process (relying upon an *Ex parte* Reuben, 128 USPQ 440, Board of Patent Appeals 1959). The undersigned finds nothing in the *Ex parte* Reuben case, nor in the MPEP, regarding the Examiner's assertion of "splitting one step into two". Regardless, independent claims 36 and 37 have been amended to recite that the forming of the insulative sidewall spacer on only one of the subject sides, and not on the other, during the one anisotropic etching step is conducted by masking the other side with masking material during the one anisotropic etching step. Support for the same is inherent in Applicant's application as-filed, for example at p.7, Ins.1-12 and in Figs. 8 and 9. Clearly, nowhere does Lee disclose any processing wherein, in a single anisotropic etching step, an anisotropically etched spacer is formed on one side of a line of floating gates and not on the other. Accordingly, even accepting the Examiner's assertion, it certainly does not suggest or disclose doing so utilizing masking material over one such side and not the other.

The Examiner is reminded that all claim limitations must be taught or suggested by the reference or references in question. It is respectfully asserted that the added limitation can in no way be inferred or suggested by modification of the Lee reference as such a limitation is simply not present or suggested.

Applicant's dependent claims 40 and 41 should be allowed as depending from allowable base claims, and for their own recited features, which are neither shown nor suggested in the cited art.

New dependent claims 55-60 are added. Such commonly recite that the line of floating gates is formed over channel active area. Further, the forming of the line of floating gates is recited as comprising providing a gate dielectric layer intermediate floating gate material and the channel active area. Further, the forming of the line of floating gates is recited to comprise initially etching through the gate dielectric layer on the source side and not on the drain side. Support for the same is inherent from Applicant's application as-filed, for example at Fig. 7 and in the specification at p.15, Ins.1-11. Accordingly, no new matter is added. The recited features are not shown or suggested in the art of record. Accordingly, added claims 55-60 should be allowed as depending from allowable base claims, and for their own recited features which are neither shown nor suggested in the cited art.

The undersigned submitted a Supplemental Information Disclosure Statement with its RCE filing on September 30, 2002. However in the last action, the undersigned did not receive an initialed copy of the PTO-1449 which was submitted with that Disclosure Statement. A duplicate copy of

the PTO-1449 is included herewith. Perhaps, the PTO-1449 was initialed, but not mailed to Applicant. Regardless, it is respectfully requested that the Examiner send the undersigned a copy of the initialed PTO-1449.

This application is believed to be in immediate condition for allowance, and action to that end is requested

Respectfully submitted,

Dated: 1-28-03

By: 
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Reg. No. 32,268

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MISS-003SERIAL NO.
09/758,878LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
Graham WolstenholmeFILING DATE
January 23, 2001GROUP
2812

U.S. PATENT DOCUMENTS

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
AA	6,235,582	05/2001	Chen	438	257	
AB	5,987,573	11/1999	Hiraka	711	156	
AC	6,232,181	05/2001	Lee	438	257	
AD	5,512,504	04/1998	Wolstenholme, et al.	437	43	
AE	6,337,244 B1	01/2002	Prall et al.	438	257	
AF	6,406,959 B2	06/2002	Prall et al.	438	258	
AG						
AH						
AI						
AJ						
AK						
AL						

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
AL							
AM							
AN							
AO							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	AP		
	AQ		
	AR		

EXAMINER .

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/768,878
 Filing Date January 23, 2001
 Inventor Graham Wolstenholme
 Assignee Micron Quantum Devices, Inc.
 Group Art Unit 2812
 Examiner Richard A. Booth
 Attorney Docket No. MI55-003
 Title Methods of Forming a Line of FLASH Memory Cells

VERSION WITH MARKINGS TO SHOW CHANGES MADE
ACCOMPANYING RESPONSE TO DECEMBER 19, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

36. (Twice Amended) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side, the line of floating gates having an insulative cap having an outermost surface;

depositing an insulative sidewall forming layer over the line of floating gates;
and

in one anisotropic etching step of the insulative sidewall forming layer, forming an insulative sidewall spacer on only the drain side and not on the source side by masking the source side with masking material during the one anisotropic etching step, the insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface.

37. (Twice Amended) A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side, the line of floating gates having an insulative cap having an outermost surface;

depositing an insulative sidewall forming layer over the line of floating gates;

in one anisotropic etching step of the insulative sidewall forming layer, forming a first insulative sidewall spacer on only one of the source side and the drain side and not the other by masking the other with masking material during the one anisotropic etching step, the first insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface; and

further comprising in another anisotropic etching step, forming a second insulative sidewall spacer on the other side, the second insulative sidewall spacer having an outermost surface which is substantially elevationally coincident with the insulative cap outermost surface.

Claims 55-60 are added.

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